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Abstract
In this thesis, a Sigma-Delta modulator (SDM) and a Sigma-Delta demodulator (SDDM) for a speech codec system are proposed. Basically, the switched-capacitor (SC) technique and the switched-current (SI) technique can be used to implement SDMs. In this thesis, the SI technique is employed.

With the SI technique, the signal processing blocks including anti-aliasing filter, ADC, DAC, reconstruction filter and logic circuits can be integrated by a standard digital CMOS process. The advantages are not only easier designed and integrated with other parts in a mixed-mode system but also lower cost than the SC technique. Besides, it is beneficial to the low voltage and low power applications. However, the encountered problem is the performance far away from the SC technique. The main reason is that the non-ideal effects will degrade the performance of SI systems. Thus, a high performance SI memory cell is needed for SI circuits and systems.

By taking into account the non-ideal effects, we develop a novel switched-current class AB memory cell and apply it on an SDM. Our memory cell has the advantages of high input dynamic range, high linearity, signal-independent settling behavior, and low power consumption. The proposed SDM is simulated with the TSMC 0.35μm 1P4M standard CMOS technology. Simulation results show that the SDM has a peak signal-to-noise plus distortion ratio (PSNDR) of 69dB, the power consumption is 0.52mW, and the dynamic range is 70dB with a single 2.5V power supply.

As to the Sigma-Delta demodulator (SDDM), it is a third-order SDDM. It encodes a 18-bit input to a 1-bit output at a clock rate of 512 kHz i.e. the oversampling ratio (OSR) is equal to 64. It has a peak-signal-to-noise-ratio (PSNR) of 82dB.

Both of the proposed SDM and SDDM are applicable to the speech codec systems with a 10-bit resolution.
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